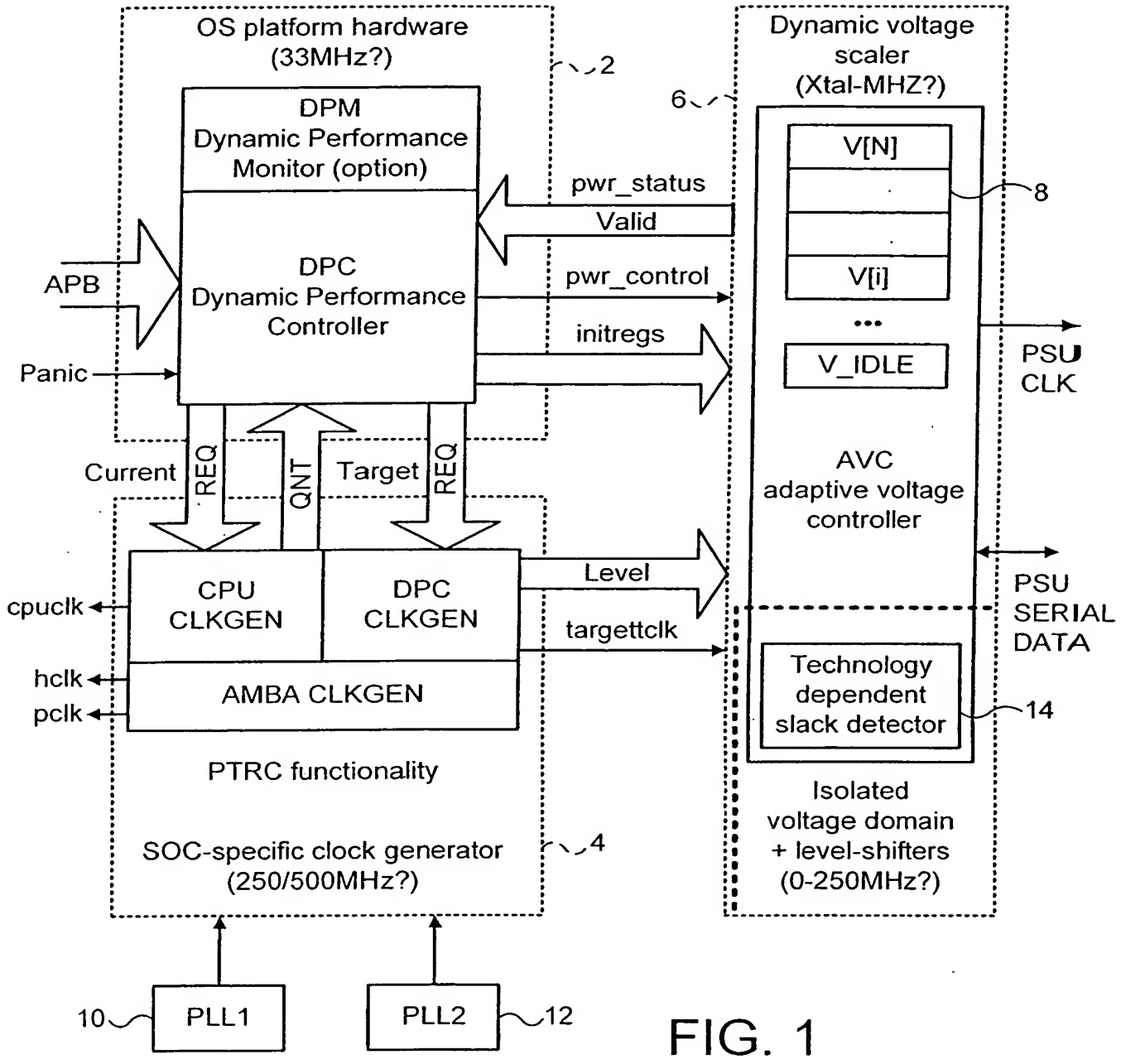

OS platform hardware
(33MHz?)
2
DPM
Dynamic Performance
Monitor (option)
DPC
Dynamic Performance
Controller
APB
Panic
pwr_status
Valid
pwr_control
initregs
Dynamic voltage
scaler
(Xtal-MHZ?)
6
V[N]
V[i]
V_IDLE
8
PSU
CLK
AVC
adaptive voltage
controller
PSU
SERIAL
DATA
Current
REQ
QNT
Target
REQ
CPU
CLKGEN
DPC
CLKGEN
Level
targettclk
cpuclk
hclk
pclk
AMBA CLKGEN
Technology
dependent
slack detector
14
PTRC functionality
Isolated
voltage domain
+ level-shifters
(0-250MHz?)
SOC-specific clock generator
(250/500MHz?)
4
10
PLL1
PLL2
12

FIG. 1

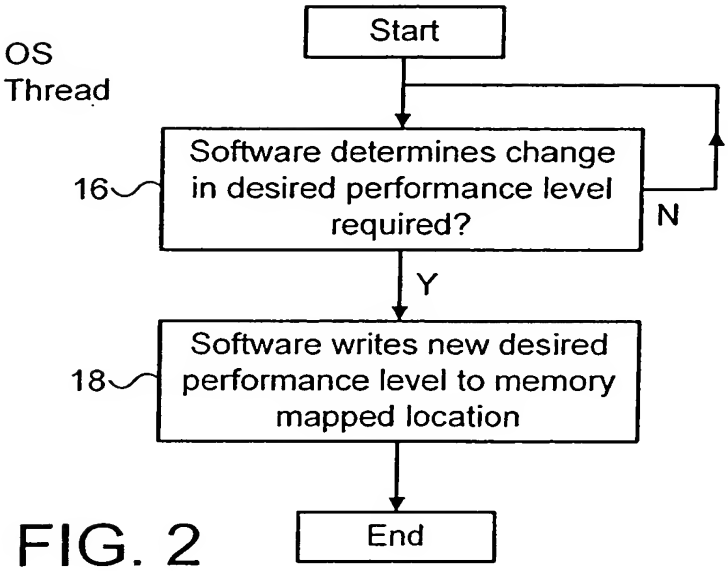


FIG. 2

Desired performance 6-bit	Control signal value	
0	00000000	Idle
1-4	00000001	
5-8	00000011	
9-12	00000111	
13-16	00001111	
17-20	00011111	
21-24	00111111	
25-28	01111111	
29-32	11111111	

Example mapping

FIG. 3

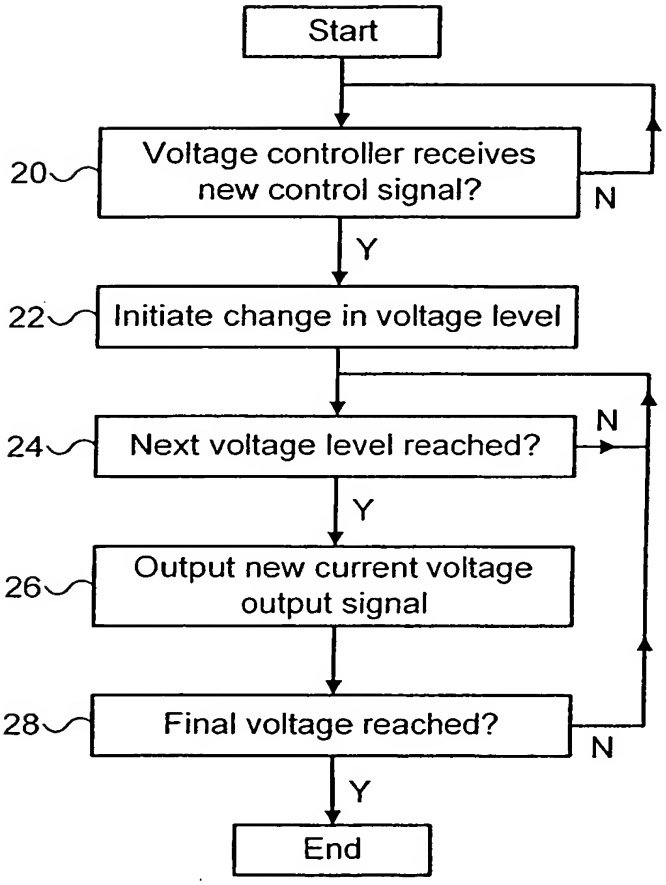
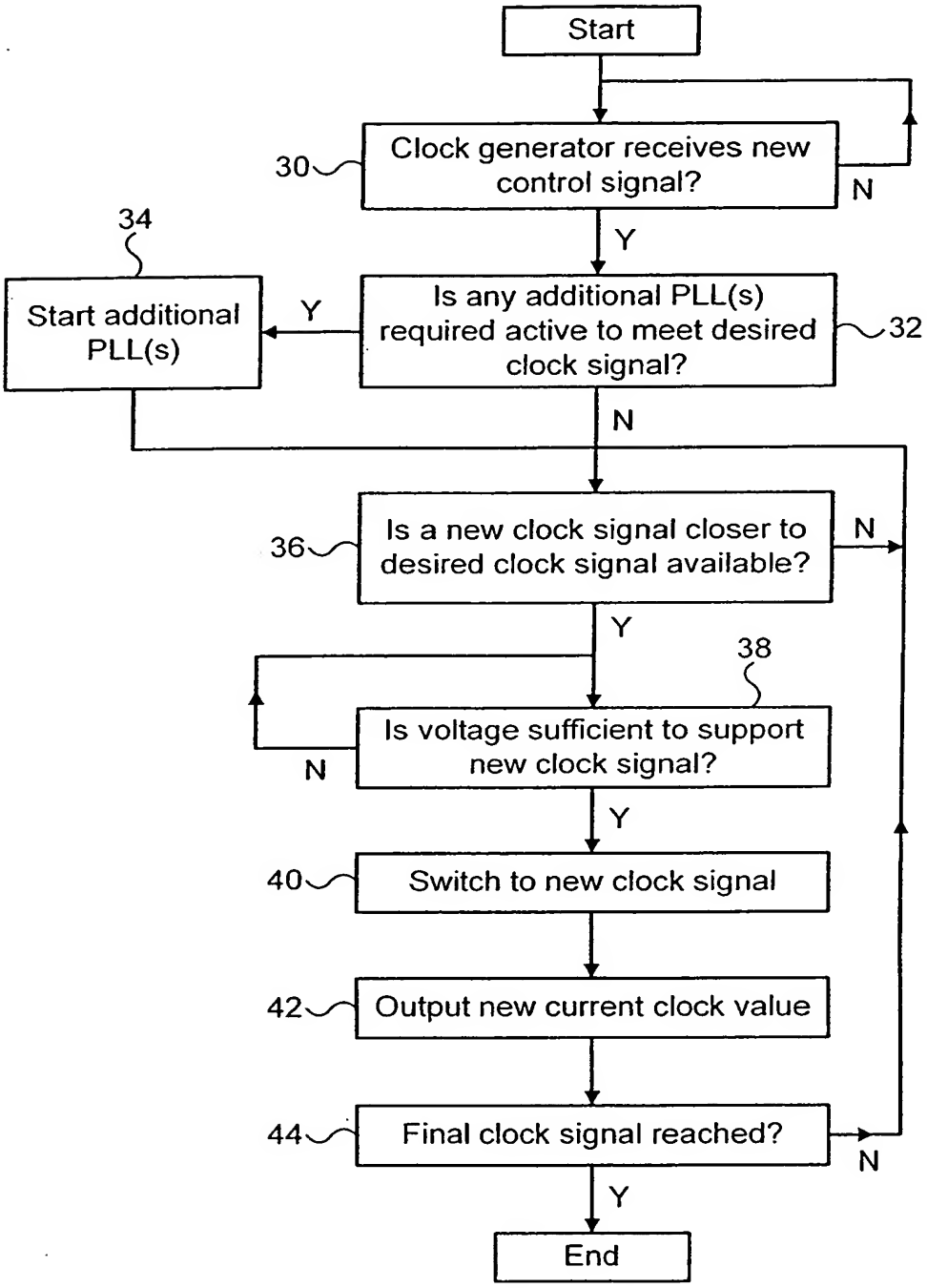

Start
20
Voltage controller receives new control signal?
N
Y
22
Initiate change in voltage level
24
Next voltage level reached?
N
Y
26
Output new current voltage output signal
28
Final voltage reached?
N
Y
End
Voltage controller

FIG. 4



CPU clock generator

FIG. 5

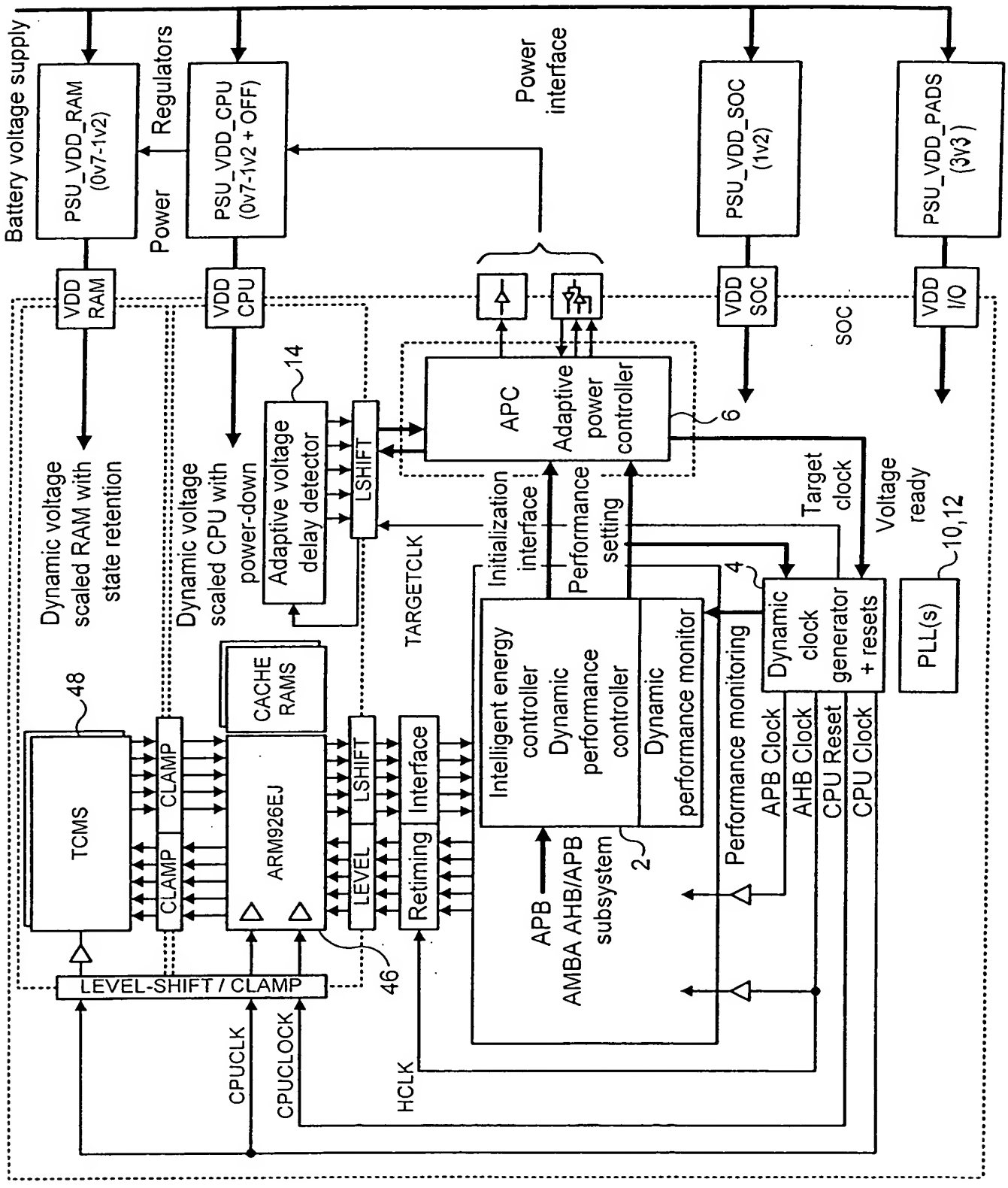

Battery voltage supply
PSU_VDD_RAM (0v7-1v2)
Regulators
Power
PSU_VDD_CPU (0v7-1v2 + OFF)
Power interface
PSU_VDD_SOC (1v2)
PSU_VDD_PADS (3v3)
VDD RAM
VDD CPU
VDD SOC
VDD I/O
SOC
Dynamic voltage scaled RAM with state retention
Dynamic voltage scaled CPU with power-down
Adaptive voltage delay detector
14
LSHIFT
APC
Adaptive power controller
6
Initialization interface
Performance setting
Target clock
Voltage ready
10,12
TARGETCLK
4
48
CACHE RAMS
TCMS
CLAMP
CLAMP
ARM926EJ
LSHIFT
LEVEL
Retiming
Interface
Intelligent energy controller
Dynamic performance controller
Dynamic performance monitor
Dynamic clock generator + resets
PLL(s)
Performance monitoring
APB Clock
AHB Clock
CPU Reset
CPU Clock
APB
AMBA AHB/APB subsystem
2
LEVEL-SHIFT / CLAMP
46
CPUCLK
CPUCLOCK
HCLK

FIG. 6

Perf/32	Binary	Fractional	%	Coding	Note
32	1.00000	1.00000	100.0%	11111111111111111111111111111111	MAX
31	0.11111	0.96875	96.9%	01111111111111111111111111111111	
30	0.11110	0.93750	93.8%	00111111111111111111111111111111	
29	0.11101	0.90625	90.6%	00011111111111111111111111111111	
28	0.11100	0.87500	87.5%	00001111111111111111111111111111	
27	0.11011	0.84375	84.4%	00000111111111111111111111111111	
26	0.11010	0.81250	81.3%	00000011111111111111111111111111	
25	0.11001	0.78125	78.1%	00000001111111111111111111111111	
24	0.11000	0.75000	75.0%	00000000111111111111111111111111	
23	0.10111	0.71875	71.9%	00000000011111111111111111111111	
22	0.10110	0.68750	68.8%	00000000001111111111111111111111	
21	0.10101	0.65625	65.6%	00000000000111111111111111111111	
20	0.10100	0.62500	62.5%	00000000000011111111111111111111	
19	0.10011	0.59375	59.4%	00000000000001111111111111111111	
18	0.10010	0.56250	56.3%	00000000000000111111111111111111	
17	0.10001	0.53125	53.1%	00000000000000011111111111111111	
16	0.10000	0.50000	50.0%	00000000000000001111111111111111	
15	0.01111	0.46875	46.9%	00000000000000000111111111111111	
14	0.01110	0.43750	43.8%	00000000000000000011111111111111	
13	0.01101	0.40625	40.6%	00000000000000000001111111111111	
12	0.01100	0.37500	37.5%	00000000000000000000111111111111	
11	0.01011	0.34375	34.4%	00000000000000000000011111111111	
10	0.01010	0.31250	31.3%	00000000000000000000001111111111	
9	0.01001	0.28125	28.1%	00000000000000000000000111111111	
8	0.01000	0.25000	25.0%	00000000000000000000000011111111	
7	0.00111	0.21875	21.9%	00000000000000000000000001111111	
6	0.00110	0.18750	18.8%	00000000000000000000000000111111	
5	0.00101	0.15625	15.6%	00000000000000000000000000011111	
4	0.00100	0.12500	12.5%	00000000000000000000000000001111	
3	0.00011	0.09375	9.4%	00000000000000000000000000000111	
2	0.00010	0.06250	6.3%	00000000000000000000000000000011	
1	0.00001	0.03125	3.1%	00000000000000000000000000000001	
0	0.00000	0.00000	0.0%	00000000000000000000000000000000	IDLE

FIG. 7

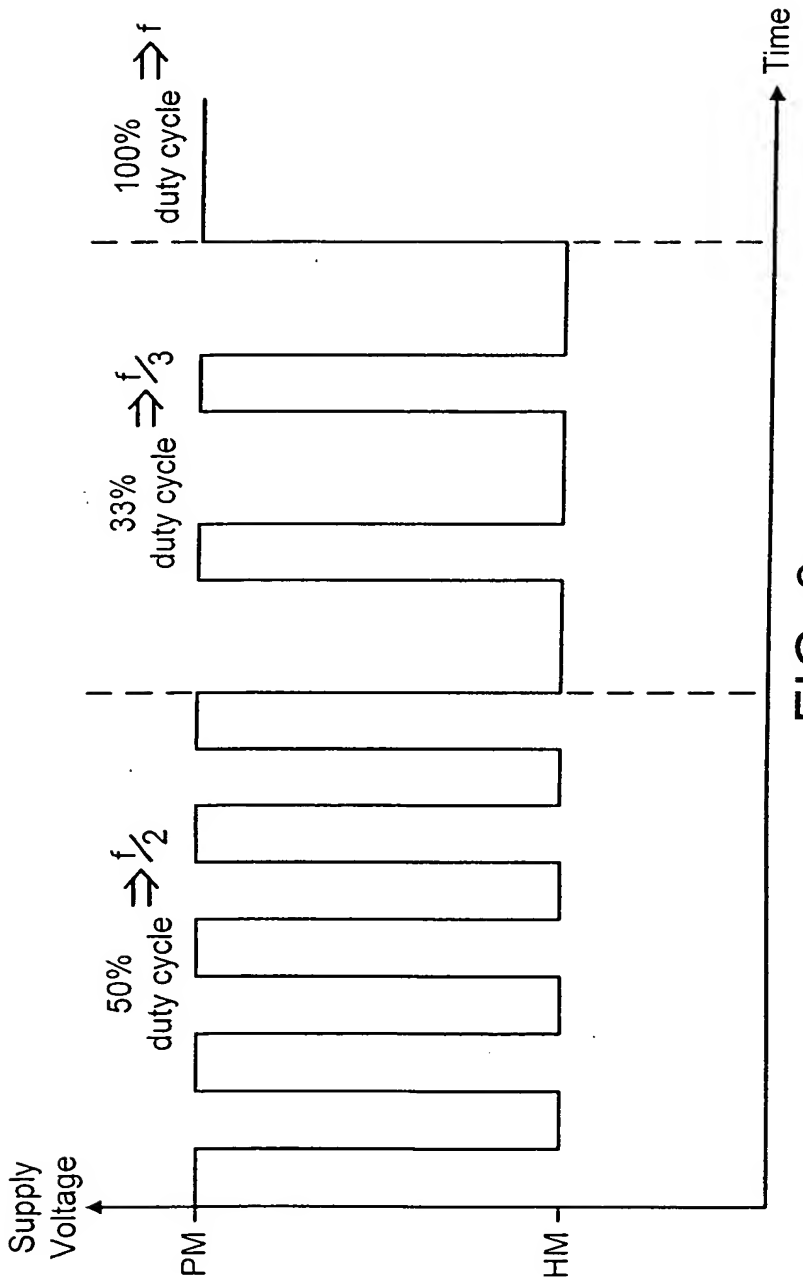

Supply Voltage
PM
HM
Time
50% duty cycle ⇒ f/2
33% duty cycle ⇒ f/3
100% duty cycle ⇒ f

FIG. 8

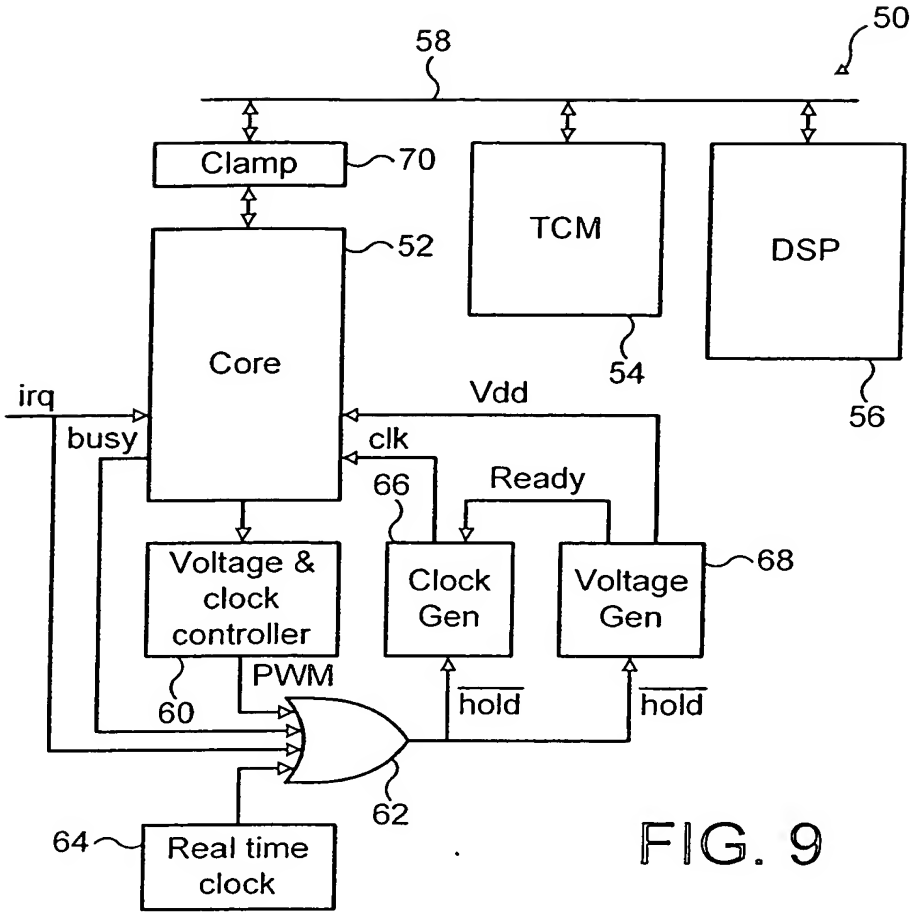

50
58
Clamp
70
TCM
DSP
52
Core
54
56
irq
busy
Vdd
clk
66
Ready
Voltage & clock controller
Clock Gen
Voltage Gen
68
PWM
60
hold
hold
62
64
Real time clock

FIG. 9

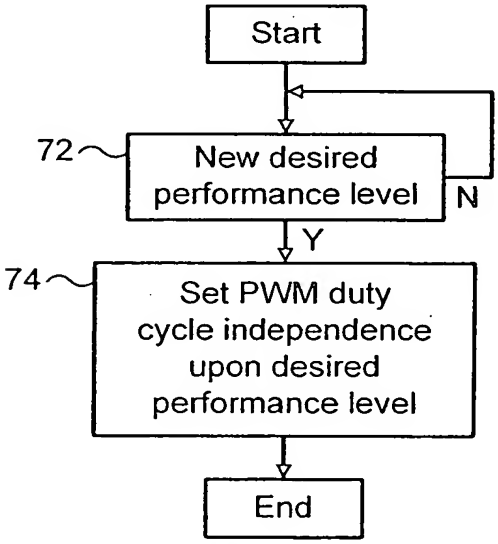

Start
72
New desired performance level
N
Y
74
Set PWM duty cycle independence upon desired performance level
End

FIG. 10

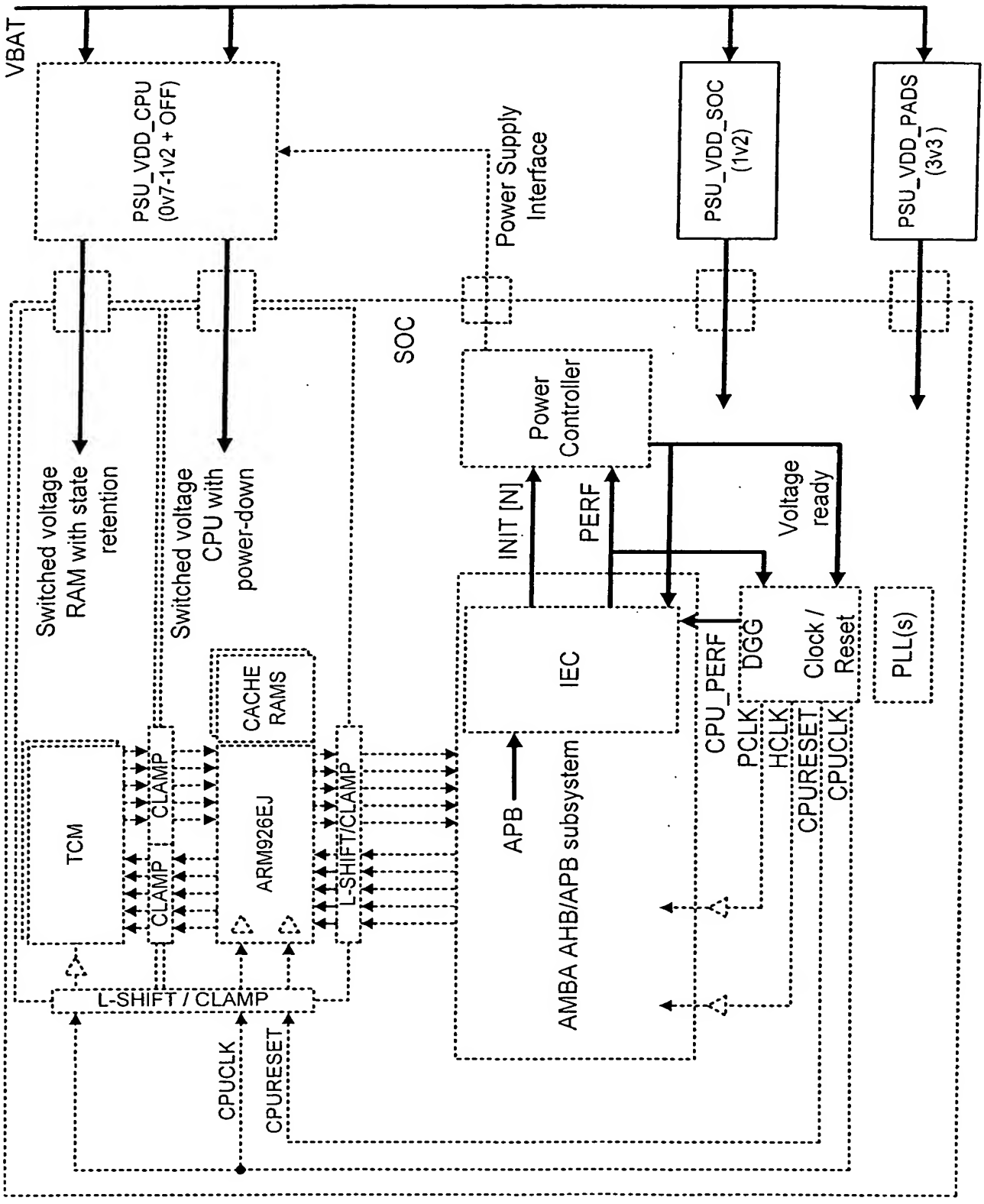

VBAT
PSU_VDD_CPU (0v7-1v2 + OFF)
PSU_VDD_SOC (1v2)
PSU_VDD_PADS (3v3)
Power Supply Interface
SOC
Switched voltage RAM with state retention
Switched voltage CPU with power-down
Power Controller
INIT [N]
PERF
Voltage ready
CACHE RAMS
TCM
CLAMP
CLAMP
ARM926EJ
L-SHIFT/CLAMP
IEC
APB
AMBA AHB/APB subsystem
CPU_PERF
DGG
Clock / Reset
PLL(s)
PCLK
HCLK
CPURESET
CPUCLK
L-SHIFT / CLAMP
CPUCLK
CPURESET

FIG. 11

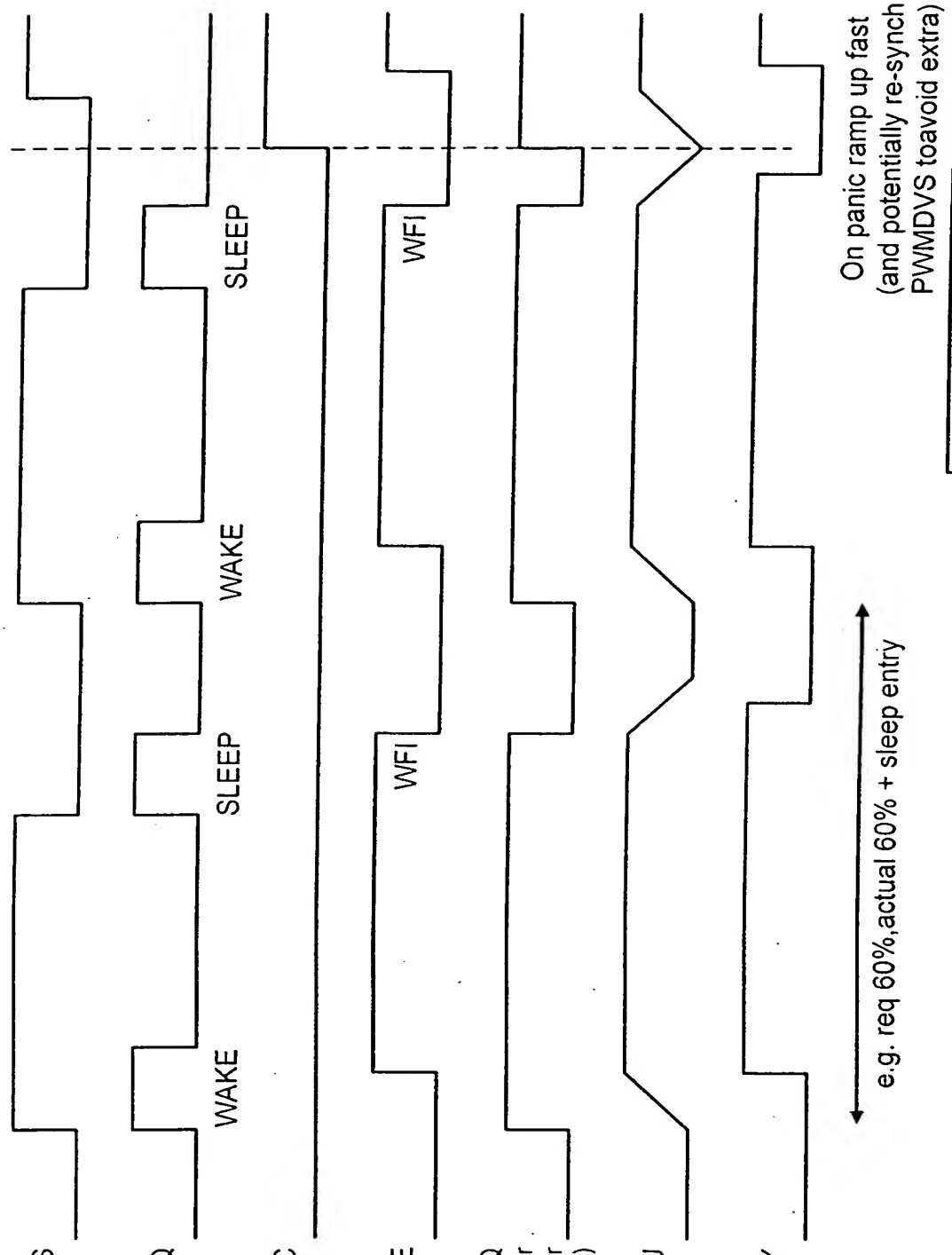

PWMDVS
IEC REQ
IEC PANIC
CPUACTIVE
VDDREQ
(PWMDVS or
CPUACTIVE or
PANIC)
VDD CPU
VREADY
WAKE
SLEEP
WAKE
SLEEP
WFI
WFI
On panic ramp up fast
(and potentially re-synch
PWMDVS toavoid extra)
PWMDVS_waves_A01
e.g. req 60%,actual 60% + sleep entry
Time slots >= 100us, 8/16/32 typically

FIG. 12